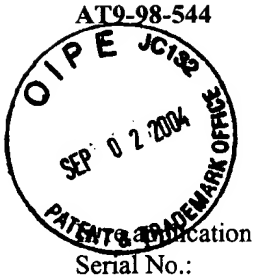
AF/2124

AT9-98-544

PATENT IFW



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Balaram Sinharoy
Serial No.: 09/435,070 Art Unit: 2124
Filed: November 4, 1999 Examiner: William H. Wood
For: CIRCUITS, SYSTEMS AND METHODS FOR PERFORMING BRANCH PREDICTIONS BY SELECTIVELY ACCESSING BIMODAL AND FETCH-BASED HISTORY TABLES

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION - 37 CFR 1.192)

1. Transmitted herewith in triplicate is the APPEAL BRIEF in this application with respect to the Notice of Appeal filed on July 28, 2004.

NOTE: "The appellant shall, within 2 months from the date of the notice of appeal under § 1.191 in an application, reissue application, or patent under reexamination, or within the time allowed for response to the action appealed from, if such time is later, file a brief in triplicate." 37 CFR 1.192(a) (emphasis added).

2. STATUS OF APPLICANT

This application is on behalf of

☒ other than a small entity

☐ small entity

verified statement:

☐ attached

☐ already filed

3. FEE FOR FILING APPEAL BRIEF

Pursuant to 37 CFR 1.17(f) the fee for filing the Appeal Brief is:

☐ small entity	$165.00
☒ other than a small entity	$330.00
Appeal Brief fee due	**$330.00**

CERTIFICATE OF MAILING (37 CFR § 1.8)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: 8/31/04

Serena Beller
(Type or print name of person mailing paper)

Serena Beller
(Signature of person mailing paper)

7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum, six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

☒ If any additional extension and/or fee is required, this is a request therefor and to charge Account No. 09-0447 (AT9-98-544).

AND/OR

☒ If any additional fee for claims is required, charge Account No. 09-0447 (AT9-98-544).

Reg. No.: 47,159

SIGNATURE OF ATTORNEY

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Austin_1 257267v.1

4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of § 1.136 for patent applications. 37 CFR 1.191(d). Also see Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply.

(complete (a) or (b) as applicable)

(a) ☐ Applicants petition for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

Extension (months)	Fee for other than small entity	Fee for small entity
☐ one month	$ 110.00	$ 55.00
☐ two months	$ 410.00	$ 205.00
☐ three months	$ 930.00	$ 465.00
☐ four months	$ 1,450.00	$ 725.00
Fee		

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request $_____

or

(b) ☒ Applicants believe that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicants have inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal Brief fee $330.00

Extension fee (if any) $0

TOTAL FEE DUE $330.00

6. FEE PAYMENT

☐ Attached is a check in the sum of $____

☒ Charge Account No. 09-0447 (AT9-98-544) the sum of $330.00.

A duplicate of this transmittal is attached.

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Balaram Sinharoy	:	Before the Examiner: William H. Wood
Serial No.: 09/435,070	:	Group Art Unit: 2124
Filed: November 4, 1999	:	
Title: CIRCUITS, SYSTEMS AND METHODS FOR PERFORMING BRANCH PREDICTIONS BY SELECTIVELY ACCESSING BIMODAL AND FETCH-BASED HISTORY TABLES	:	IBM Corporation Intellectual Property Law 11400 Burnet Road Austin, Texas 78758

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation, which is the assignee of the entire right, title and interest in the above-identified patent application.

CERTIFICATION UNDER 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on August 31, 2004.

Serena Beller
Signature

Serena Beller
(Printed name of person certifying)

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant, Appellant's legal representative or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 10 and 21-40 are pending in the Application. Claims 10 and 21-40 stand rejected.

IV. STATUS OF AMENDMENTS

Appellant's response to the Office Action having the mailing date of February 13, 2004, has been considered, but the Examiner indicated that it did not place the application in condition for allowance because Appellant's arguments were deemed unpersuasive.

V. SUMMARY OF INVENTION

A branch prediction apparatus in accordance with a preferred embodiment of the present inventive concepts includes three tables are used for branch prediction, namely, a local branch history table (LBHT), a fetch-based branch history table (GBHT) and a selector table (GSEL). Specification, page 9, lines 13-18. In the illustrated embodiment, each table is composed of a preselected number, *n*, of entries each of which includes a number, *p*, of 1-bit counters. Specification, page 9, lines 18-20. For purposes of the present discussion, when a given one of the counters in the local or fetch-based branch history tables is set to a Logic 1, that counter (entry) will be considered as being set to a taken branch prediction value. Specification, page 9, lines 20-22. Consequently, in this configuration, a counter (entry) storing a Logic 0 will be considered as storing a branch not-taken-prediction bit. Specification, page 9, line 22 through page 10, line 1. It should be noted however, that in alternate

embodiments, the reverse logic may be used without deviating from the inventive concepts. Specification, page 10, lines 1-3.

The local branch history table is accessed for obtaining branch predictions using a pointer constituting *n* bits taken from the current cache line address, in instruction fetch address register (IFAR) in a conventional fashion. Specification, page 10, lines 4-6. Fetch-based branch history table is accessed for obtaining branch predictions in a fashion in which *n* number of bits taken from the current cache line address are bitwise XORed with *n* number of bits from GHV register. Specification, page 10, lines 6-10.

In the preferred embodiment, the entries of GSEL are accessed for obtaining predictions using the same pointer generated for the fetch-based branch history table. Specification, page 10, lines 13-15. The accessed entry from selector table is then used by selection logic to select either the local branch prediction values output from LBHT or the fetch-based branch prediction value accessed from GBHT for use as the final branch prediction value for determining if the branch is to be taken or not taken. Specification, page 10, lines 15-19. Note that a number *q* of the prediction values may be from LBHT and a remaining number *p-q* may be from GBHT. Specification, page 10, lines 21-22. Thus, the number of predictions in an entry accommodates all of the instructions that are fetched in a single cycle, which may be referred to as a fetch group (FG). Specification, page 11, lines 1-3. The number, *p*, of instructions in a fetch group may be eight in an embodiment of the present invention. Specification, page 11, lines 1-3.

The GHV tracks the history of branch instructions as they are fetched and executed. Specification, page 11, lines 10-11. Thus, as branches are executed and resolved, the GHV is updated. Specification, page 11, lines 11-12.

Additionally, the entries in the LBHT, GBHT and GSEL 30 must also be updated in response to the execution of branch instructions. Specification, page 11, lines 15-16. The entries are updated by providing information to the appropriate entry in the LBHT, GBHT and GSEL for setting or resetting, as appropriate, the *p* one-bit counters in the corresponding entry, depending on the prediction and the resolution, or actual outcome, of the branch. Specification, page 11, lines 16-20.

In this way, branch prediction based on a prediction history is implemented having a constant amount of processing. Specification, page 28, lines 15-16. According to the principles of the present invention, one bit is shifted into the global history vector for each fetch group. Specification, page 28, lines 16-17. The loading of a bit, "one" or a "zero," in the global history vector essentially captures the path the program has taken to reach the branch instruction being predicted, and thereby provides an indication of how the branch will behave (taken or not-taken). Specification, page 28, lines 16-17.

VI. ISSUE

A. Are claims 10 and 30 properly rejected under 35 U.S.C. §103(a) as being unpatentable over Patt et al. ("Alternative Implementations of Hybrid Branch Predictors") (hereinafter "Patt") in view of Talcott et al. (U.S. Patent No. 6,289,441) (hereinafter "Talcott") and in further view of Shimomura et al. (U.S. Patent No. 5,737,381) (hereinafter "Shimomura")?

B. Are claims 28-29 and 31-39 properly rejected under 35 U.S.C. §103(a) as being unpatentable over Patt in view of Talcott?

C. Are claims 21-27 and 40 properly rejected under 35 U.S.C. §103(a) as being unpatentable over Patt in view of Talcott and in further view of McFarling ("Combining Branch Predictors")?

VII. GROUPING OF CLAIMS

Claims 10 and 30 form a first group.

Claims 28 and 31-33 form a second group.

Claims 23 and 40 form a third group.

Claims 38 and 39 form a fourth group.

Claims 21, 22, 24, 25, 26, 27, 29, 34, 35, 36 and 37 should not be grouped together and should be considered separately.

The reasons for these groupings are set forth in Appellants' arguments in Section VIII.

VIII. ARGUMENT

A. Claims 10 and 30 are not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Patt in view of Talcott and in further view of Shimomura.

The Examiner has rejected claims 10 and 30 under 35 U.S.C. §103(a) as being unpatentable over Patt in view of Talcott and in further view of Shimomura. Paper No. 15, page 2. Appellant respectfully traverses these rejections for at least the reasons stated below.

1. The Examiner has not provided any objective evidence for combining Patt with Talcott.

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370,

55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner's motivation for modifying Patt with Talcott to have a fetch-based accessed history table, as recited in claim 10, is "to increase branch prediction accuracy for many instructions, which is increasingly necessary for superscalar pipeline designs (column 2, lines 3-7; column 1, lines 54-67)." Paper No. 13, page 3. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner's motivation is not a motivation as to why one of ordinary skill in the art with the primary reference (Patt) in front of him would have been motivated to modify the primary reference (Patt) with the teachings of the secondary reference (Talcott). There is no suggestion in Patt of having a fetch-based accessed history table (Examiner admits that Patt does not teach this limitation) in order to increase branch prediction accuracy for many instructions (Examiner's motivation). The Examiner's motivation is a motivation for the secondary reference (Talcott) to solve its problem. In fact, the Examiner cites column 2, lines 3-7 and column 1, lines 54-67 of Talcott as support for his motivation which addresses the problem to be solved by Talcott and the manner in solving that problem. Talcott teaches that one method of addressing the branch problem is acceptable for a microprocessor with a limited number of pipelines; however, as the number of pipeline increases, there is a greater chance of multiple branch instructions being processed in a fetch cycle. Column 1, lines 54-67. Talcott further teaches that the present invention offers a method and apparatus for performing multiple branch predictions per fetch cycle which allows a superscalar design with a large number of pipelines to avoid stalls when there are multiple branch instructions in a fetch bundle. Column 2, lines 1-7. Hence, the Examiner's motivation addresses the problem to be solved in Talcott. The Examiner's

motivation is not a suggestion to combine the primary reference (Patt) with the secondary reference (Talcott). The Examiner must provide objective evidence as to why one of ordinary skill in the art with the primary reference (Patt) in front of him, which teaches comparing various hybrid predictor implementations to determine which single-scheme predictor combinations and branch selection mechanisms were most effective (page 257 of Patt), would have been motivated to modify the teachings of the primary reference (Patt) with the teachings of the secondary reference (Talcott), which teaches determining which instructions in a plurality of fetch instructions are branches and whether such branches are taken or not taken thereby finding the oldest taken branch (Abstract of Talcott). *See In re Lee*, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1318 (Fed. Cir. 2000). Merely stating the motivation to solve the problem of the secondary reference (Talcott) is not evidence for suggesting the combination of the primary reference (Patt) with the secondary reference (Talcott). *See Id.* Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 10 and 30. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of combining Patt, which teaches comparing various hybrid predictor implementations to determine which single-scheme predictor combinations and branch selection mechanisms were most effective, with Talcott, which teaches determining which instructions in a plurality of fetch instructions are branches and whether such branches are taken or not taken thereby finding the oldest taken branch. *Id.* There is no suggestion in Patt of determining which instructions in a plurality of fetch instructions are branches. Neither is there any suggestion in Patt of determining which instructions in a plurality of fetch instructions are branches and whether such branches are taken or not taken. Neither is there any suggestion in Patt of determining which instructions in a plurality of fetch instructions are branches and whether such branches are taken or not taken thereby finding the oldest taken branch.

Since the Examiner has not submitted objective evidence for modifying Patt with Talcott, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 10 and 30. *Id.*

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Patt to have a fetch-based accessed history table (Examiner admits that Patt does not teach this limitation). *Id.* There is no suggestion in Patt of having a fetch-based accessed history table. Since the Examiner has not submitted objective evidence for modifying Patt to have a fetch-based accessed history table, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 10 and 30. *Id.*

Further, the Examiner's motivation for modifying Patt with Shimomura to have each entry in the table comprise a 1-bit counter, as recited in claim 10 and similarly in claim 30, is "to implement a simple design structure for easy understanding or implement less hardware to save space and thus money (Talcott: column 4, lines 15-19, implementing a counter for each instruction would imply a need to save space and cost, by using less hardware)." Paper No. 13, page 4. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner's motivation is not a motivation as to why one of ordinary skill in the art with the primary reference (Patt) in front of him would have been motivated to modify the primary reference (Patt) with the teachings of the secondary reference (Shimomura). There is no suggestion in Patt of having each entry in the tables comprise a 1-bit counter (Examiner admits that Patt does not teach this limitation) in order to implement a simple design structure for easy understanding or to implement less hardware to save space and money (Examiner's motivation). The Examiner's motivation is not a motivation to modify Patt to have each entry in the table comprise a 1-bit counter. The Examiner's motivation relates to the number of branch prediction

table counters (each branch prediction counter corresponds to two instructions within the current fetch bundle) that are necessary to determine if the branch is taken or not taken. Column 4, lines 2-9 of Talcott. The greater the number of counters the greater the accuracy; however, the greater the number of counters the greater the hardware cost. Column 4, lines 15-19 of Talcott. In fact, the Examiner cites to this passage in Talcott as support for his motivation. This language does not address as to why one of ordinary skill in the art would modify Patt to have each entry in the tables comprise a 1-bit counter. There is no language in the cited passages that suggests having each entry in the tables comprise a 1-bit counter in order to implement a simple design structure for easy understanding or to implement less hardware to save space and money. Further, the Examiner has not provided any basis in fact and/or technical reasoning to support the assertion that having a 1-bit counter in each entry in the tables is a simple design structure or saves space or money. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that having a 1-bit counter in each entry in the tables is a simple design structure or saves space or money, and that it be so recognized for persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745, 49 U.S.P.Q.2d 1949, 1950-51 (Fed. Cir. 1999). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 10 and 30. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of combining Patt, which teaches comparing various hybrid predictor implementations to determine which single-scheme predictor combinations and branch selection mechanisms were most effective, with Shimomura, which teaches a counting device that includes a carry/borrow signal to be supplied from a one-bit counter to another one-bit counter in the subsequent stage that is inputted to an input/cutoff element such as an AND circuit (Abstract of Shimomura). *Id.* There is no suggestion in Patt of having a counting device that

includes a carry/borrow signal. Neither is there any suggestion in Patt of having a counting device that includes a carry/borrow signal to be supplied from a one-bit counter to another one-bit counter in the subsequent stage. Neither is there any suggestion in Patt of having a counting device that includes a carry/borrow signal to be supplied from a one-bit counter to another one-bit counter in the subsequent stage that is inputted to an input/cutoff element such as an AND circuit. Since the Examiner has not submitted objective evidence for modifying Patt with Shimomura, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 10 and 30. *Id.*

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Patt to have each entry in the tables comprise a 1-bit counter (Examiner admits that Patt does not teach this limitation). *Id.* There is no suggestion in Patt of having each entry in the tables comprise a 1-bit counter. Since the Examiner has not submitted objective evidence for modifying Patt to have each entry in the tables comprise a 1-bit counter, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 10 and 30. *Id.*

Further, as stated above, the Examine modified Patt with Shimomura to have each entry in the tables comprise a 1-bit counter, as recited in claim 10 and similarly in claim 30. The Examiner asserts that a two-bit counter "naturally comprises" a one-bit counter, and that Shimomura is evidence that it was known at the time of the invention to implement one-bit counters. Paper No. 13. page 3. The Appellant respectfully disagrees that a two-bit counter comprises a one-bit counter.[1] The Appellant has previously addressed this assertion in detail. *See e.g.* Applicant's Second Rely Under 37 C.F.R. § 1.111, mailed September 5, 2003, (hereinafter, the

1 As the Appellant previously noted, this statement is similar to asserting that a bicycle "comprises" a unicycle. A bicycle is not two unicycles nor does a bicycle "teach" two unicycles because it has two wheels where a unicycle has one wheel. Similarly, a 2-bit counter does not comprise two 1-bit counters.

"Applicant's Second Reply," page 5.) A two-bit counter has two output bits that are correlated. A one-bit counter has a single output bit, and two one-bit counters have two single output bits, that is the output bits are uncorrelated. The Examiner's assertion is tantamount to stating that the value "10" comprises the value "1" or, equivalently, the value "0," which is contrary to common knowledge. Contrary to PTO practice, the Examiner has yet to address the substance of the Appellant's showings. *See* M.P.E.P. § 707.07(f). This is not to say that a two-bit counter cannot be fabricated from one-bit counters and the appropriate interconnections. However, it would be appreciated by persons of ordinary skill in the art that the result is an integral device that is different than two one-bit counters, which have a different truth table than the two-bit counter. Thus, it is immaterial that Shimomura discloses a one-bit counter. Thus, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 10 and 30. *Id.*

As a result of the foregoing, Appellants respectfully assert that the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 10 and 30. M.P.E.P. §2143.

2. By combining Patt with Shimomura, the principle of operation of Patt would change.

If the proposed modification or combination of the prior art would change the principle of the operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959). Further, if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). For the reasons discussed below, Appellant submits that by modifying Patt to use 1-bit counters (Examiner's proposed modification), the principle of operation in Patt would

change and subsequently render the operation of Patt to perform its purpose unsatisfactorily.

Patt explicitly teaches that the Branch Prediction Selection Table (BPST) used in the two-level prediction scheme is a table of two-bit counters just as disclosed in conjunction with the hybrid prediction scheme. Section 4.2, pages 255-56. Patt further teaches that the BPST records which predictor was most frequently correct for the times this branch occurred with the associated branch history. Section 4.1, page 255. Patt further teaches that this second level of history keeps track of the more accurate predictor for branches at different branch execution states. *Id.* Patt further teaches that when a branch is fetched, its instruction address and the current branch history are used to hash into the BPST. *Id.* Patt further teaches that the associated counter is then used to select the appropriate prediction. *Id.* Patt further teaches that by using the branch history to distinguish more execution states, 2-level predictor selection scheme can more accurately select the appropriate predictions. *Id.* Patt further teaches that the BPST is a 1K entry table of two bit counters. Section 4.2, page 256. Patt further illustrates the various performances of various 2-level BPS mechanisms. *Id.* As illustrated in Figure 4 of Patt, a 1K-entry of two bit counters is superior over other 2-level BPS mechanisms, e.g., gshare.

The Examiner has not provided any basis in fact and/or technical reasoning to support the assertion that the BPST, as taught in Patt, could be replaced with a 1K entry table of 1-bit counters and that Patt would still be able to perform its operation satisfactorily. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). Since a 1-bit counter is cheaper to implement than a 2-bit counter, one would assume that Patt would have taught that the BPST has a 1K-entry of 1-bit counters everything being equal. However, Patt specifically taught that the BPST has a 1K-entry of 2-bit counters instead of 1-bit counters presumably to reduce the misprediction rate at a greater rate. That is, the Examiner must provide extrinsic evidence that must make

clear that by replacing the 2-bit counter with a 1-bit counter in each entry in the BPST that the misprediction rate would not increase thereby causing Patt to perform its purpose unsatisfactory. The Examiner has not provided such evidence. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 10 and 30. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959); *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984).

B. Claims 28-29 and 31-39 are not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Patt in view of Talcott.

The Examiner has rejected claims 28-29 and 31-39 under 35 U.S.C. §103(a) as being unpatentable over Patt in view of Talcott. Paper No. 15, page 4. Appellant respectfully traverses these rejections for at least the reasons stated below.

1. The Examiner has not provided any objective evidence for combining Patt with Talcott.

As stated above, a *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner's motivation for modifying Patt with Talcott to have a second branch history table comprising a plurality of fetch-based accessed entries, as recited in claim 28 and similarly in claim 34, is "to increase branch prediction accuracy for

many instructions, which is increasingly necessary for superscalar pipeline designs (column 1, lines 54-67)." Paper No. 13, page 6. The Examiner's motivation for modifying Patt with Talcott to have entries of a selector table accessed using fetch-based accessing, as recited in claim 29, is "to increase branch prediction accuracy for many instructions, which is increasingly necessary for superscalar pipeline designs (column 1, lines 54-67)." Paper No. 13, page 6. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner's motivation is not a motivation as to why one of ordinary skill in the art with the primary reference (Patt) in front of him would have been motivated to modify the primary reference (Patt) with the teachings of the secondary reference (Talcott). There is no suggestion in Patt of having a fetch-based accessed history table in order to increase branch prediction accuracy for many instructions (Examiner's motivation). The Examiner's motivation is a motivation for the secondary reference (Talcott) to solve its problem. In fact, the Examiner cites column 1, lines 54-67 of Talcott as support for his motivation which addresses the problem to be solved by Talcott and the manner in solving that problem. Talcott teaches that one method of addressing the branch problem is acceptable for a microprocessor with a limited number of pipelines; however, as the number of pipeline increases, there is a greater chance of multiple branch instructions being processed in a fetch cycle. Column 1, lines 54-67. Talcott further teaches that the present invention offers a method and apparatus for performing multiple branch predictions per fetch cycle which allows a superscalar design with a large number of pipelines to avoid stalls when there are multiple branch instructions in a fetch bundle. Column 2, lines 1-7. Hence, the Examiner's motivation addresses the problem to be solved in Talcott. The Examiner's motivation is not a suggestion to combine the primary reference (Patt) with the secondary reference (Talcott). The Examiner must provide objective evidence as to why one of ordinary skill in the art with the primary reference (Patt) in

front of him, which teaches comparing various hybrid predictor implementations to determine which single-scheme predictor combinations and branch selection mechanisms were most effective (page 257 of Patt), would have been motivated to modify the teachings of the primary reference (Patt) with the teachings of the secondary reference (Talcott), which teaches determining which instructions in a plurality of fetch instructions are branches and whether such branches are taken or not taken thereby finding the oldest taken branch (Abstract of Talcott). *See In re Lee*, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1318 (Fed. Cir. 2000). Merely stating the motivation to solve the problem of the secondary reference (Talcott) is not evidence for suggesting the combination of the primary reference (Patt) with the secondary reference (Talcott). *See Id.* Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 28-29 and 31-39. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of combining Patt, which teaches comparing various hybrid predictor implementations to determine which single-scheme predictor combinations and branch selection mechanisms were most effective, with Talcott, which teaches determining which instructions in a plurality of fetch instructions are branches and whether such branches are taken or not taken thereby finding the oldest taken branch. *Id.* There is no suggestion in Patt of determining which instructions in a plurality of fetch instructions are branches. Neither is there any suggestion in Patt of determining which instructions in a plurality of fetch instructions are branches and whether such branches are taken or not taken. Neither is there any suggestion in Patt of determining which instructions in a plurality of fetch instructions are branches and whether such branches are taken or not taken thereby finding the oldest taken branch. Since the Examiner has not submitted objective evidence for modifying Patt with

Talcott, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 28-29 and 31-39. *Id.*

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Patt to have a fetch-based accessed history table (Examiner admits that Patt does not teach this limitation). *Id.* There is no suggestion in Patt of having a fetch-based accessed history table. Since the Examiner has not submitted objective evidence for modifying Patt to have a fetch-based accessed history table, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 28-29 and 31-39. *Id.*

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Patt to have entries of a selector table accessed using fetch-based accessing (Examiner admits that Patt does not teach this limitation). *Id.* There is no suggestion in Patt of using fetch-based accessing. Neither is there any suggestion of having entries of a selector table accessed using fetch-based accessing. Since the Examiner has not submitted objective evidence for modifying Patt to have entries of a selector table accessed using fetch-based accessing, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 29. *Id.*

Further, the Examiner's motivation for modifying Patt and Talcott to have a sum of a number of bits in the first set of branch prediction bits and a number of bits in the second set of branch prediction bits not less than a number of instructions in a fetch group, as recited in claim 34, is "to develop systems of reduced instruction throughput to alleviate complexity." Paper No. 13, page 9. The Examiner further states that "this implementation would have been obvious because one of ordinary skill in the art would recognize the most straight-forward (easiest) implementation (an entry in both tables containing values for all instructions in the fetch group) would in

effect have a sum greater (no less than) than the number of instructions in a fetch group." Paper No. 13, page 9. These motivations are insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). The Examiner must submit objective evidence in support of modifying Patt and Talcott to have a sum of a number of bits in the first set of branch prediction bits and a number of bits in the second set of branch prediction bits not less than a number of instructions in a fetch group. *Id.* There is no suggestion in either Patt or Talcott to have a sum of a number of bits in the first set of branch prediction bits and a number of bits in the second set of branch prediction bits not less than a number of instructions in a fetch group. Neither is there any suggestion in either Patt or Talcott to have a sum of a number of bits in the first set of branch prediction bits and a number of bits in the second set of branch prediction bits not less than a number of instructions in a fetch group in order to reduce instruction throughput (Examiner's motivation). Neither is there any suggestion in either Patt or Talcott to have a sum of a number of bits in the first set of branch prediction bits and a number of bits in the second set of branch prediction bits not less than a number of instructions in a fetch group in order to have the most straight forward implementation (Examiner's motivation). The Examiner's motivations do not address as to why one of ordinary skill in the art with the teachings of Patt and Talcott in front of him would have been motivated to modify the teachings of Patt and Talcott to have a sum of a number of bits in the first set of branch prediction bits and a number of bits in the second set of branch prediction bits not less than a number of instructions in a fetch group. M.P.E.P. §2143. Furthermore, the Examiner has not provided any objective evidence as to the source of such motivations. *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1457-58 (Fed. Cir. 1998). The Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of

obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claim 34. *Id.*

Further, the Examiner's motivation for modifying Patt and Talcott to update the current selector table entry to a logic value associated with the fetch-based branch history table when neither of corresponding bits of the first and second sets of branch prediction bits correctly predicts the branch resolution outcome, as recited in claim 37, is "to gradually adjust the predictor to the more likely correct future choice, especially if there is no evidence not to make such an adjustment (i.e. neither predictor providing accurate)." Paper No. 134, pages 11-12. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). The Examiner must submit objective evidence in support of modifying Patt and Talcott to update a current selector table entry to a logic value associated with the fetch-based branch history table when neither of corresponding bits of the first and second sets of branch prediction bits correctly predicts the branch resolution outcome. *Id.* There is no suggestion in either Patt or Talcott to update a current selector table entry to a logic value associated with the fetch-based branch history table when neither of corresponding bits of the first and second sets of branch prediction bits correctly predicts the branch resolution outcome. Neither is there any suggestion in either Patt or Talcott to update a current selector table entry to a logic value associated with the fetch-based branch history table when neither of corresponding bits of the first and second sets of branch prediction bits correctly predicts the branch resolution outcome in order to gradually adjust the predictor to the more likely correct future choice (Examiner's motivation). The

Examiner's motivation does not address as to why one of ordinary skill in the art with the teachings of Patt and Talcott in front of him would have been motivated to modify the teachings of Patt and Talcott to update a current selector table entry to a logic value associated with the fetch-based branch history table when neither of corresponding bits of the first and second sets of branch prediction bits correctly predicts the branch resolution outcome. M.P.E.P. §2143. Furthermore, the Examiner has not provided any objective evidence as to the source of such motivations. *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1457-58 (Fed. Cir. 1998). The Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claim 37. *Id.*

As a result of the foregoing, Appellant respectfully asserts that the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 28-29 and 31-39. M.P.E.P. §2143.

2. Patt and Talcott, taken singly or in combination, do not teach or suggest the following claim limitations.

Appellant respectfully asserts that Patt and Talcott, taken singly or in combination, do not teach or suggest "wherein a sum of a number of bits in the first set of branch prediction bits and a number of bits in the second set of branch prediction bits is not less than a number of instructions in a fetch group" as recited in claim 34. The Examiner admits that neither Patt nor Talcott teach or suggest these limitations. Paper No. 13, page 13. Moreover, Talcott explicitly teaches a mechanism where the number of prediction counter values is less than the number of instructions in a fetch bundle. Column 3, lines 67-68. Furthermore the references would not be expected to teach such a limitation because Patt did not consider the prediction of multiple branches, and Talcott does not consider combined predictors.

Nevertheless, the Examiner concludes that it would have been obvious that "if one bit came from the first table and one bit came from the second table it would be not less than the instructions in a fetch group if that group were composed of two instructions." Paper No. 13, page 9. Appellant respectfully asserts that there is no teaching in either of the references, nor is there a recitation in the claim to which it pertains. There is no teaching in either of the references that suggests a first bit coming from a first table and a second bit coming from a second table. The Examiner is relying solely on knowledge gleaned from the Appellant's disclosure which is impermissible. *In re McLaughlin*, 443 F.2d 1392, 1395, 170 U.S.P.Q. 209, 212 (C.C.P.A. 1971). Therefore, the Examiner has not presented a *prima facie* case of obviousness, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Appellant further asserts that Patt and Talcott, taken singly or in combination, do not teach or suggest "wherein the step of updating the selector table comprises the substeps of: determining if at least one of the first set of branch prediction bits correctly predicts the corresponding branch resolution outcome; updating the corresponding entry in the selector table to a first logic value when the at least one of the first set of prediction bits correctly represents the branch resolution outcome; determining if at least one of the second set of branch prediction bits correctly predicts the branch resolution outcome; and updating the corresponding entry in the selector table to a second logic value when the at least one of the second set of branch prediction bits correctly represents the branch resolution outcome " as recited in claim 35. The Examiner cites page 252, section 2 of Patt as teaching the above-cited claim limitations. Paper No. 13, pages 9-10. The Examiner further cites Figure 2 of Patt as teaching the above-cited claim limitations. Paper No. 13, page 22. Appellant respectfully traverses and asserts that Patt instead teaches that each static branch was associated with a counter which would keep track of which predictor was currently

more accurate for that branch. Patt further teaches that upon confirmation of a branch prediction, the counter would be incremented or decremented depending on which single-scheme predictor was correct. Patt further teaches that if both were correct (or incorrect), the counter state would be left unchanged. As understood by the Appellant, Patt further teaches than an entry in the Branch Predictor Selection Table is used to select one of two possible predictions. However, there is no language in the cited passage that teaches a first and a second set of branch prediction bits. Neither does Patt teach that the Branch Predictor Selection Table (assuming the Examiner is asserting that the Branch Predictor Selection Table teaches a selector table) is updated. There is no language in Patt of updating an entry in the Branch Predictor Selection Table to a particular logic value when a prediction bit retrieved from a bimodal branch history table correctly represents the branch resolution outcome. Neither is there any language in Patt of updating an entry in the Branch Predictor Selection Table to a particular logic value when a prediction bit retrieved from a fetch-based branch history table correctly represents the branch resolution outcome. Therefore, the Examiner has not presented a *prima facie* case of obviousness, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Appellant further asserts that Patt and Talcott, taken singly or in combination, do not teach or suggest "determining if at least one bit of both the first and second sets of branch history bits correctly predict the branch resolution outcome; maintaining the current value of corresponding bits in the corresponding selector table entry when the at least one bit of both the first and second sets of branch prediction bits correctly predict the branch resolution outcome; determining if at least one bit of both the first and second sets of branch prediction bits incorrectly predict the branch resolution outcome; and maintaining the current value of corresponding bits in the corresponding selector table entry when the at least one bit of both the first and second sets of branch history bits incorrectly predict the branch history outcome"

as recited in claim 36. The Examiner cites page 252, section 2 of Patt as teaching the above-cited claim limitations. Paper No. 13, pages 10-11. The Examiner further cites Figure 2 of Patt as teaching the above-cited claim limitations. Paper No. 13, page 22. Appellant respectfully traverses and asserts that Patt instead teaches that each static branch was associated with a counter which would keep track of which predictor was currently more accurate for that branch. Patt further teaches that upon confirmation of a branch prediction, the counter would be incremented or decremented depending on which single-scheme predictor was correct. Patt further teaches that if both were correct (or incorrect), the counter state would be left unchanged. As understood by the Appellant, Patt further teaches than an entry in the Branch Predictor Selection Table is used to select one of two possible predictions. However, there is no language in the cited passage that teaches a first and a second set of branch prediction bits. Neither does Patt teach maintaining the current value of a bit in an entry in the Branch Predictor Selection Table entry (assuming the Examiner is asserting that the Branch Predictor Selection Table teaches a selector table) when a prediction bit retrieved from either the bimodal branch history table or the fetch-based branch history table correctly predicts the branch resolution outcome. Neither is there any language in Patt of maintaining the current value of a bit in a Branch Predictor Selection Table entry when a prediction bit retrieved from either the bimodal branch history table or the fetch-based branch history table incorrectly predicts the branch history outcome. Therefore, the Examiner has not presented a *prima facie* case of obviousness, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Appellant further asserts that Patt and Talcott, taken singly or in combination, do not teach or suggest "determining whether at least one bit of both the first and second sets of branch prediction bits correctly predict the branch resolution outcome; maintaining the current value of corresponding bits in the corresponding selector

table entry when at the least one bit of both the first and second sets of branch prediction bits correctly predict the branch resolution outcome" as recited in claim 37. The Examiner cites page 252, section 2 of Patt as teaching the above-cited claim limitations. Paper No. 13, page 11. The Examiner further cites Figure 2 of Patt as teaching the above-cited claim limitations. Paper No. 13, page 22. Appellant respectfully traverses and asserts that Patt instead teaches that each static branch was associated with a counter which would keep track of which predictor was currently more accurate for that branch. Patt further teaches that upon confirmation of a branch prediction, the counter would be incremented or decremented depending on which single-scheme predictor was correct. Patt further teaches that if both were correct (or incorrect), the counter state would be left unchanged. As understood by the Appellant, Patt further teaches than an entry in the Branch Predictor Selection Table is used to select one of two possible predictions. However, there is no language in the cited passage that teaches a first and a second set of branch prediction bits. Neither does Patt teach maintaining the current value of a bit in an entry in the Branch Predictor Selection Table entry (assuming the Examiner is asserting that the Branch Predictor Selection Table teaches a selector table) when a prediction bit retrieved from both the bimodal branch history table and the fetch-based branch history table correctly predicts the branch resolution outcome. Therefore, the Examiner has not presented a *prima facie* case of obviousness, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Appellant further asserts that Patt and Talcott, taken singly or in combination, do not teach or suggest "wherein said step of accessing the fetch-based branch history table comprises the substep of generating an address from at least some bits of a branching instruction and bits retrieved from a history register" as recited in claim 38. The Examiner cites page 253, fourth bulleted item of Patt as teaching the above-cited claim limitation. Paper No. 13, page 12. Appellant respectfully traverses and asserts

that Patt instead teaches that the gshare(m) single-scheme predictors consists of a single m-bit global branch history and a single pattern history table. Patt further teaches that the branch history and the branch address are XORed together to form the index into the pattern history table. There is no language in the cited passage that teaches accessing a fetch-based branch history table. Neither is there any language in the cited passage that teaches generating an address. Instead, Patt teaches XORing together a branch address and a branch history. Further, there is no language in the cited passage that teaches generating an address from at least some bits of a branching instruction. Neither is there any language in the cited passage that teaches generating an address from at least some bits retrieved from a history register. Therefore, the Examiner has not presented a *prima facie* case of obviousness, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

As a result of the foregoing, Appellant respectfully asserts that there are numerous claim limitations not taught or suggested in the cited prior art, and thus the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 28-29 and 31-39. M.P.E.P. §2143.

C. Claims 21-27 and 40 are not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Patt in view of Talcott and in further view of McFarling.

The Examiner has rejected claims 21-27 and 40 under 35 U.S.C. §103(a) as being unpatentable over Patt in view of Talcott and in further view of McFarling. Paper No. 13, page 12. Appellant respectfully traverses these rejections for at least the reasons stated below.

1. The Examiner has not provided any objective evidence for combining Patt with Talcott and McFarling.

As stated above, a *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner's motivation for modifying Patt with Talcott to have a fetch-based accessed history table where each entry is operable for containing bits representing a prediction value for a plurality of branches in a fetch group, as recited in claim 21, is "to increase branch prediction accuracy for many instructions, which is increasingly necessary for superscalar pipeline designs (column 2, lines 3-7; column 1, lines 54-67)." Paper No. 13, page 14. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner's motivation is not a motivation as to why one of ordinary skill in the art with the primary reference (Patt) in front of him would have been motivated to modify the primary reference (Patt) with the teachings of the secondary reference (Talcott). There is no suggestion in Patt of having a fetch-based accessed history table in order to increase branch prediction accuracy for many instructions (Examiner's motivation). The Examiner's motivation is a motivation for the secondary reference (Talcott) to solve its problem. In fact, the Examiner cites column 2, lines 3-7 and column 1, lines 54-67 of Talcott as support for his motivation which

addresses the problem to be solved by Talcott and the manner in solving that problem. Talcott teaches that one method of addressing the branch problem is acceptable for a microprocessor with a limited number of pipelines; however, as the number of pipeline increases, there is a greater chance of multiple branch instructions being processed in a fetch cycle. Column 1, lines 54-67. Talcott further teaches that the present invention offers a method and apparatus for performing multiple branch predictions per fetch cycle which allows a superscalar design with a large number of pipelines to avoid stalls when there are multiple branch instructions in a fetch bundle. Column 2, lines 1-7. Hence, the Examiner's motivation addresses the problem to be solved in Talcott. The Examiner's motivation is not a suggestion to combine the primary reference (Patt) with the secondary reference (Talcott). The Examiner must provide objective evidence as to why one of ordinary skill in the art with the primary reference (Patt) in front of him, which teaches comparing various hybrid predictor implementations to determine which single-scheme predictor combinations and branch selection mechanisms were most effective (page 257 of Patt), would have been motivated to modify the teachings of the primary reference (Patt) with the teachings of the secondary reference (Talcott), which teaches determining which instructions in a plurality of fetch instructions are branches and whether such branches are taken or not taken thereby finding the oldest taken branch (Abstract of Talcott). *See In re Lee*, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1318 (Fed. Cir. 2000). Merely stating the motivation to solve the problem of the secondary reference (Talcott) is not evidence for suggesting the combination of the primary reference (Patt) with the secondary reference (Talcott). *See Id.* Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 21-27. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of combining Patt, which teaches comparing various

hybrid predictor implementations to determine which single-scheme predictor combinations and branch selection mechanisms were most effective, with Talcott, which teaches determining which instructions in a plurality of fetch instructions are branches and whether such branches are taken or not taken thereby finding the oldest taken branch. *Id.* There is no suggestion in Patt of determining which instructions in a plurality of fetch instructions are branches. Neither is there any suggestion in Patt of determining which instructions in a plurality of fetch instructions are branches and whether such branches are taken or not taken. Neither is there any suggestion in Patt of determining which instructions in a plurality of fetch instructions are branches and whether such branches are taken or not taken thereby finding the oldest taken branch. Since the Examiner has not submitted objective evidence for modifying Patt with Talcott, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 21-27. *Id.*

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Patt to have a fetch-based accessed history table where each entry is operable for containing bits representing a prediction value for a plurality of branches in a fetch group (Examiner admits that Patt does not teach this limitation). *Id.* There is no suggestion in Patt of having a fetch-based accessed history table. Neither is there any suggestion in Patt of having a fetch-based accessed history table where each entry is operable for containing bits representing a prediction value. Neither is there any suggestion in Patt of having a fetch-based accessed history table where each entry is operable for containing bits representing a prediction value for a plurality of branches in a fetch group. Since the Examiner has not submitted objective evidence for modifying Patt to have a fetch-based accessed history table where each entry is operable for containing bits representing a prediction value for a plurality of branches in a fetch group, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 21-27. *Id.*

Further, the Examiner simply cites column 1, line 63 – column 2, line 10 of Talcott as motivation for modifying Patt with McFarling to have each fetch group represented by a bit in the history register, as recited in claim 21. Paper No. 13, page 14. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner's motivation is not a motivation as to why one of ordinary skill in the art with the primary reference (Patt) in front of him would have been motivated to modify the primary reference (Patt) with the teachings of the secondary references (Talcott and McFarling). The Examiner's motivation is a motivation for the secondary reference (Talcott) to solve its problem. In fact, the Examiner cites column 1, line 63 – column 2, 10 of Talcott as support for his motivation which addresses the problem to be solved by Talcott and the manner in solving that problem. Talcott teaches that one method of addressing the branch problem is acceptable for a microprocessor with a limited number of pipelines; however, as the number of pipeline increases, there is a greater chance of multiple branch instructions being processed in a fetch cycle. Column 1, lines 54-67. Talcott further teaches that the present invention offers a method and apparatus for performing multiple branch predictions per fetch cycle which allows a superscalar design with a large number of pipelines to avoid stalls when there are multiple branch instructions in a fetch bundle. Column 2, lines 1-7. Hence, the Examiner's motivation addresses the problem to be solved in Talcott. The Examiner's motivation is not a suggestion to combine the primary reference (Patt) with the secondary references (Talcott and McFarling). The Examiner must provide objective evidence as to why one of ordinary skill in the art with the primary reference (Patt) in front of him, which teaches comparing various hybrid predictor implementations to determine which single-scheme predictor combinations and branch selection mechanisms were most effective (page 257 of Patt), would have been motivated to modify the teachings of the primary reference (Patt) with the teachings of the secondary reference (Talcott), which teaches

determining which instructions in a plurality of fetch instructions are branches and whether such branches are taken or not taken thereby finding the oldest taken branch (Abstract of Talcott), along with the teachings of the other secondary reference (McFarling), which teaches using a bit-wise exclusive OR of the global branch history and the branch address to access predictor counters results in better performance for a given counter array size (page 16 of McFarling). *See In re Lee*, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1318 (Fed. Cir. 2000). Merely stating the motivation to solve the problem of the secondary reference (Talcott) is not evidence for suggesting the combination of the primary reference (Patt) with the secondary references (Talcott and McFarling). *See Id.* Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 21-27. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of combining Patt, which teaches comparing various hybrid predictor implementations to determine which single-scheme predictor combinations and branch selection mechanisms were most effective, with McFarling, which teaches using a bit-wise exclusive OR of the global branch history and the branch address to access predictor counters results in better performance for a given counter array size. *Id.* There is no suggestion in Patt of using a bit-wise exclusive OR of the global branch history and the branch address. Neither is there any suggestion in Patt of using a bit-wise exclusive OR of the global branch history and the branch address to access predictor counters. Since the Examiner has not submitted objective evidence for modifying Patt with McFarling, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 21-27. *Id.*

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Patt to have each fetch group represented

by a bit in the history register (Examiner admits that Patt does not teach this limitation). *Id.* There is no suggestion in Patt of having a fetch group. Neither is there any suggestion in Patt of having each fetch group represented by a bit in a history register. Since the Examiner has not submitted objective evidence for modifying Patt to have each fetch group represented by a bit in the history register, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 21-27. *Id.*

Further, the Examiner's motivation for modifying Patt, Talcott and McFarling to set a corresponding entry in each of said bimodal and fetch-based branch history tables to a first value when a branch is taken at branch resolution time; and set a corresponding entry in each of said bimodal and fetch-based branch history tables to a second value when a branch is not taken at branch resolution time, as recited in claim 22, is "to provide an accurate history as to which type of single predictor is correct in order to be more successful in future predictions." Paper No. 13, page 15. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). The Examiner must submit objective evidence in support of modifying Patt, Talcott and McFarling to set a corresponding entry in each of said bimodal and fetch-based branch history tables to a first value when a branch is taken at branch resolution time and to set a corresponding entry in each of said bimodal and fetch-based branch history tables to a second value when a branch is not taken at branch resolution time. *Id.* There is no suggestion in either Patt or Talcott or McFarling to set a corresponding entry in each of said bimodal and fetch-based branch history tables to a first value when a branch is taken at branch resolution time and to set a corresponding entry in each of said bimodal and fetch-based branch

history tables to a second value when a branch is not taken at branch resolution time. Neither is there any suggestion in either Patt or Talcott or McFarling to set a corresponding entry in each of said bimodal and fetch-based branch history tables to a first value when a branch is taken at branch resolution time and to set a corresponding entry in each of said bimodal and fetch-based branch history tables to a second value when a branch is not taken at branch resolution time in order to provide an accurate history as to which type of single predictor is correct in order to be more successful in future predictions (Examiner's motivation). The Examiner's motivation does not address as to why one of ordinary skill in the art with the teachings of Patt, Talcott and McFarling in front of him would have been motivated to modify the teachings of Patt, Talcott and McFarling to set a corresponding entry in each of said bimodal and fetch-based branch history tables to a first value when a branch is taken at branch resolution time and to set a corresponding entry in each of said bimodal and fetch-based branch history tables to a second value when a branch is not taken at branch resolution time. M.P.E.P. §2143. Furthermore, the Examiner has not provided any objective evidence as to the source of such a motivation. *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1457-58 (Fed. Cir. 1998). The Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claim 22. *Id.*

Further, the Examiner's motivation for modifying Patt and Talcott with McFarling to have history register which comprises a shift register and have the branch prediction circuitry further comprise circuitry for updating a shift register by shifting in a preselected prediction value for each fetch group, as recited in claim 23 and similarly in claim 40, is "to make use of existing (and thus well understood) technology when implementing hybrid branch predictors." Paper No. 13, page 16.

The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). The Examiner must submit objective evidence in support of modifying Patt and Talcott with McFarling to have history register which comprises a shift register and have the branch prediction circuitry further comprise circuitry for updating a shift register by shifting in a preselected prediction value for each fetch group. *Id.* There is no suggestion in either Patt or Talcott or McFarling to have history register which comprises a shift register and have the branch prediction circuitry further comprise circuitry for updating a shift register by shifting in a preselected prediction value for each fetch group. Neither is there any suggestion in either Patt or Talcott or McFarling to have history register which comprises a shift register and have the branch prediction circuitry further comprise circuitry for updating a shift register by shifting in a preselected prediction value for each fetch group to make use of existing (and thus well understood) technology when implementing hybrid branch predictors (Examiner's motivation). The Examiner's motivation does not address as to why one of ordinary skill in the art with the teachings of Patt, Talcott and McFarling in front of him would have been motivated to modify the teachings of Patt and Talcott with McFarling to have history register which comprises a shift register and have the branch prediction circuitry further comprise circuitry for updating a shift register by shifting in a preselected prediction value for each fetch group. M.P.E.P. §2143. Furthermore, the Examiner has not provided any objective evidence as to the source of such a motivation. *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1457-58 (Fed. Cir. 1998). The Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir.

2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 23 and 40. *Id.*

Further, the Examiner's motivation for modifying Patt, Talcott and McFarling to set a value in a selected entry in the selector table to a value associated with the fetch-based table when corresponding values from the bimodal and fetch based branch history tables both do not correctly predict a corresponding branch resolution outcome, as recited in claim 27, is "to gradually adjust the predictor to the more likely correct future choice, especially if there is no evidence not to make such an adjustment." Paper No. 13, page 18. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). The Examiner must submit objective evidence in support of modifying Patt, Talcott and McFarling to set a value in a selected entry in the selector table to a value associated with the fetch-based table when corresponding values from the bimodal and fetch based branch history tables both do not correctly predict a corresponding branch resolution outcome. *Id.* There is no suggestion in either Patt or Talcott or McFarling to set a value in a selected entry in the selector table to a value associated with the fetch-based table when corresponding values from the bimodal and fetch based branch history tables both do not correctly predict a corresponding branch resolution outcome. Neither is there any suggestion in either Patt or Talcott or McFarling to set a value in a selected entry in the selector table to a value associated with the fetch-based table when corresponding values from the bimodal and fetch based branch history tables both do not correctly predict a corresponding branch resolution outcome in order to gradually adjust the predictor to the more likely correct future choice, especially if there is no evidence not to make such an adjustment (Examiner's motivation). The Examiner's motivation does not

address as to why one of ordinary skill in the art with the teachings of Patt, Talcott and McFarling in front of him would have been motivated to modify the teachings of Patt, Talcott and McFarling to set a value in a selected entry in the selector table to a value associated with the fetch-based table when corresponding values from the bimodal and fetch based branch history tables both do not correctly predict a corresponding branch resolution outcome. M.P.E.P. §2143. Furthermore, the Examiner has not provided any objective evidence as to the source of such a motivation. *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1457-58 (Fed. Cir. 1998). The Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claim 27. *Id.*

As a result of the foregoing, Appellants respectfully assert that the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 21-27 and 40. M.P.E.P. §2143.

2. Patt, Talcott and McFarling, taken singly or in combination, do not teach or suggest the following claim limitations.

Appellant respectfully asserts that Patt, Talcott and McFarling, taken singly or in combination, do not teach or suggest "a fetch-based branch history table comprising a plurality of entries for storing a prediction value and accessed by a pointer generated from selected bits of said branch address and bits from a history register, each entry of the fetch-based branch history table operable for containing bits representing a prediction value for a plurality of branches in a fetch group" as recited in claim 21. The Examiner cites column 3, line 58 – column 4, line 25 of Talcott as teaching the above-cited claim limitation. Paper No. 13, page 13. Appellant respectfully traverses and asserts that Talcott instead teaches that the Branch Prediction Table provides eight counters where each counter corresponds to an

instruction in a fetch bundle. However, there is no language in the cited passage that teaches that the Branch Prediction Table includes entries for storing a prediction value that are accessed by a pointer generated from selected bits of a branch address and bits from a history register. Neither is there any language in the cited passages that teaches that the Branch Prediction Table includes entries for storing a prediction value that are accessed by a pointer generated from selected bits of a branch address and bits from a history register where each entry of the Branch Prediction Table is operable for containing bits representing a prediction value for a plurality of branches in a fetch group. Instead, Talcott teaches having a counter corresponding to an instruction in a fetch bundle. This is not the same as an entry containing bits representing a prediction value for a plurality of branches in a fetch group. Therefore, the Examiner has not presented a *prima facie* case of obviousness, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Appellant further asserts that Patt, Talcott and McFarling, taken singly or in combination, do not teach or suggest "wherein each fetch group is represented by a bit in the history register" as recited in claim 21. The Examiner cites Figure 10 on page 12 of McFarling as teaching the above-cited claim limitation. Paper No. 13, page 14. Appellant respectfully traverses and asserts that McFarling instead teaches a single shift register GR. However, there is no language in McFarling that teaches representing a fetch group by a bit in a history register. Neither is there any language in either Patt or Talcott of representing a fetch group by a bit in a history register. Therefore, the Examiner has not presented a *prima facie* case of obviousness, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Appellant further asserts that Patt, Talcott and McFarling, taken singly or in combination, do not teach or suggest " wherein said history register comprises a shift

register and said branch prediction circuitry further comprises circuitry for updating said shift register by shifting in a preselected prediction value for each fetch group" as recited in claim 23 and similarly in claim 40. The Examiner cites page 6, section 5, first paragraph and pages 11-12, section 7 of McFarling as teaching the above-cited claim limitation. Paper No. 13, page 16. Appellant respectfully traverses and asserts that McFarling instead teaches a global shift register as well as how global history information weakly identifies the current branch. There is no language in the cited passages that teaches a updating a shift register by shifting in a preselected prediction value for each fetch group. In fact, Appellant could not identify the term "fetch" or any variation thereof in the cited passages of McFarling. Therefore, the Examiner has not presented a *prima facie* case of obviousness, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Appellant further asserts that Patt, Talcott and McFarling, taken singly or in combination, do not teach or suggest "update a corresponding bit in a selected entry in said selector table with a first value when a bimodal prediction value from said bimodal branch history table correctly represents a corresponding branch resolution; and update a corresponding bit in a selected entry in said selector table with a second value when a fetch-based prediction value from said fetch-based branch history table correctly represents the corresponding branch resolution" as recited in claim 24. The Examiner cites page 252, section 2 of Patt as teaching the above-cited claim limitation. Paper No. 13, page 16. Appellant respectfully traverses and asserts that Patt instead teaches that each static branch was associated with a counter which would keep track of which predictor was currently more accurate for that branch. Patt further teaches that upon confirmation of a branch prediction, the counter would be incremented or decremented depending on which single-scheme predictor was correct. Patt further teaches that if both were correct (or incorrect), the counter state would be left unchanged. There is no language in the cited passage of Patt that

teaches updating a bit in an entry in a selector table with a first value when a bimodal prediction value from a bimodal branch history table correctly represents a corresponding branch resolution. Neither is there any language in the cited passage of Patt that teaches updating a bit in an entry in the selector table with a second value when a fetch-based prediction value from a fetch-based branch history table correctly represents the corresponding branch resolution. Therefore, the Examiner has not presented a *prima facie* case of obviousness, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Appellant further teaches that Patt, Talcott and McFarling, taken singly or in combination, do not teach or suggest "wherein the plurality of selection bits are operable for selecting a first subset of prediction values from the bimodal branch history table and a second subset of prediction values from the fetch-based branch history table" as recited in claim 25. The Examiner cites page 252, section 2 of Patt as teaching the above-cited claim limitation. Paper No. 13, page 17. Appellant respectfully traverses and asserts that Patt instead teaches that each static branch was associated with a counter which would keep track of which predictor was currently more accurate for that branch. Patt further teaches that upon confirmation of a branch prediction, the counter would be incremented or decremented depending on which single-scheme predictor was correct. Patt further teaches that if both were correct (or incorrect), the counter state would be left unchanged. There is no language in the cited passage of Patt that teaches a plurality of selection bits operable for selecting a first subset of prediction values from a bimodal branch history table. Neither is there any language in the cited passage of Patt that teaches a plurality of selection bits operable for selecting a second subset of prediction values from a fetch-based branch history table. Therefore, the Examiner has not presented a *prima facie* case of obviousness, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Further, in connection with the rejection of the above-cited claim limitation, the Examiner had previously in the Office Action asserted that Talcott teaches a fetch-based branch history table. However, the Examiner has not presented any motivation for modifying Patt with Talcott to have a plurality of selection bits operable for selecting a second subset of prediction values from a fetch-based branch history table. The Examiner is required to provide a suggestion or motivation to modify Patt with Talcott to have a plurality of selection bits operable for selecting a second subset of prediction values from a fetch-based branch history table. M.P.E.P. §2143. As the Examiner has not provided such motivation, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 25. M.P.E.P. §2143.

Appellant further asserts that Patt, Talcott and McFarling, taken singly or in combination, do not teach or suggest "wherein said circuitry for updating said selector table is further operable to maintain a value in a selected entry in said selector table when corresponding values from said bimodal and fetch-based branch history tables both correctly represent a corresponding branch resolution, and wherein said circuitry for updating said selector table is further operable to maintain a value in a selected entry in said selector table when neither values from said bimodal and fetch-based branch history tables correctly represent a corresponding branch resolution" as recited in claim 26. The Examiner cites page 252, section 2 of Patt as teaching the above-cited claim limitation. Paper No. 13, page 17. Appellant respectfully traverses. As stated above, Patt instead teaches that each static branch was associated with a counter which would keep track of which predictor was currently more accurate for that branch. Patt further teaches that upon confirmation of a branch prediction, the counter would be incremented or decremented depending on which single-scheme predictor was correct. Patt further teaches that if both were correct (or incorrect), the counter state would be left unchanged. There is no language in the cited passage that teaches updating a selector table to maintain a value in a selected entry in the selector table when corresponding values from the bimodal and fetch-based branch history

tables both correctly represent a corresponding branch resolution. Neither is there any language in the cited passage that teaches updating the selector table to maintain a value in a selected entry in the selector table when neither values from the bimodal and fetch-based branch history tables correctly represent a corresponding branch resolution. Therefore, the Examiner has not presented a *prima facie* case of obviousness, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

As a result of the foregoing, Appellant respectfully asserts that there are numerous claim limitations not taught or suggested in the cited prior art, and thus the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 21-27 and 40. M.P.E.P. §2143.

IX. CONCLUSION

For the reasons noted above, the rejections of claims 10 and 21-40 are in error. Appellant respectfully requests reversal of the rejections and allowance of claims 10 and 21-40.

Respectfully submitted,
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APPENDIX

10. A processing system comprising:

a first branch history table comprising a plurality of bimodally accessed entries for storing a first set of branch prediction bits;

a second branch history table comprising a plurality of fetch-based accessed entries for storing a second set of branch prediction bits;

a selector for selecting in response to a selection control bit selected from a set of selection control bits, a bit from a selected one of said sets of bits accessed from said first and second branch history tables; and

a selector table comprising a plurality of entries for storing said a set of selector bits as a function of a performance history of said first and second sets of branch prediction bits stored in said first and second branch history tables, wherein said each said entry in said tables comprises a 1-bit counter.

21. Branch prediction circuitry comprising:

a bimodal branch history table comprising a plurality of entries each for storing a prediction value and accessed by selected bits of a branch address;

a fetch-based branch history table comprising a plurality of entries for storing a prediction value and accessed by a pointer generated from selected bits of said branch address and bits from a history register, each entry of the fetch-based branch history table operable for containing bits representing a prediction value for a plurality of branches in a fetch group, wherein each fetch group is represented by a bit in the history register; and

a selector table comprising a plurality of entries each for storing a plurality of selection bits and accessed by a pointer generated from selected bits from said branch address and bits from said history register, each said selector bit used for selecting between a bimodal prediction value accessed from the bimodal history table and a prediction value accessed from said fetch-based history table.

22. The branch prediction circuitry of Claim 21 and further comprising circuitry for updating said bimodal and fetch-based branch history tables operable to:

set a corresponding entry in each of said bimodal and fetch-based branch history tables to a first value when a branch is taken at branch resolution time; and

set a corresponding entry in each of said bimodal and fetch-based branch history tables to a second value when a branch is not taken at branch resolution time.

23. The branch prediction circuitry of Claim 21 wherein said history register comprises a shift register and said branch prediction circuitry further comprises circuitry for updating said shift register by shifting in a preselected prediction value for each fetch group.

24. The branch prediction circuitry of Claim 21 and further comprising circuitry for updating said selector table operable to:

update a corresponding bit in a selected entry in said selector table with a first value when a bimodal prediction value from said bimodal branch history table correctly represents a corresponding branch resolution; and

update a corresponding bit in a selected entry in said selector table with a second value when a fetch-based prediction value from said fetch-based branch history table correctly represents the corresponding branch resolution.

25. The branch prediction circuitry of Claim 21 wherein the plurality of selection bits are operable for selecting a first subset of prediction values from the bimodal branch history table and a second subset of prediction values from the fetch-based branch history table.

26. The branch prediction circuitry of Claim 23 wherein said circuitry for updating said selector table is further operable to maintain a value in a selected entry in said selector table when corresponding values from said bimodal and fetch-based

branch history tables both correctly represent a corresponding branch resolution, and wherein said circuitry for updating said selector table is further operable to maintain a value in a selected entry in said selector table when neither values from said bimodal and fetch-based branch history tables correctly represent a corresponding branch resolution.

27. The branch prediction circuitry of Claim 23 wherein said circuitry for updating said selector table is further operable to set a value in a selected entry in said selector table to a value associated with said fetch-based table when corresponding values from said bimodal and fetch based branch history tables both do not correctly predict a corresponding branch resolution outcome.

28. A processing system comprising:

a first branch history table comprising a plurality of bimodally accessed entries, each entry for storing a first set of branch prediction bits;

a second branch history table comprising a plurality of fetch-based accessed entries each entry for storing a second set of branch prediction bits;

a selector for selecting, in response to a plurality of selection control bits, a set of prediction bits from a selected one of said sets of bits accessed from said first and second branch history tables; and

a selector table comprising a plurality of entries, each entry for storing a plurality of selection control bits wherein the selection control bits are set as a function of a performance history of corresponding first and second sets of branch prediction bits stored in said first and second branch history tables.

29. The processing system of Claim 28 wherein said entries of said selector table are accessed using fetch-based accessing.

30. The processing system of Claim 28 wherein said each said entry in said tables comprises a 1-bit counter.

31. The processing system of Claim 28 wherein said first and second branch history tables and said selector table form a portion of a branch execution unit.

32. The processing system of Claim 31 wherein said branch execution unit forms a part of a microprocessor.

33. The processing system of Claim 32 and further comprising memory coupled to said microprocessor.

34. A method of performing branch predictions in a processing system including a bimodal branch history table, a fetch-based branch history table and a selector table, the method comprising the substeps of:

accessing the bimodal branch history table to retrieve a first set of branch prediction bits;

accessing the fetch-based branch history table to retrieve a set of second branch prediction bits;

selecting between the first and second sets of branch prediction bits in response to corresponding bits retrieved from the selector table, wherein a sum of a number of bits in the first set of branch prediction bits and a number of bits in the second set of branch prediction bits is not less than a number of instructions in a fetch group; and

updating the selector table as a function of actual branch resolution.

35. The method of Claim 34 wherein said step of updating the selector table comprises the substeps of:

determining if at least one of the first set of branch prediction bits correctly predicts the corresponding branch resolution outcome;

updating the corresponding entry in the selector table to a first logic value when the at least one of the first set of prediction bits correctly represents the branch resolution outcome;

determining if at least one of the second set of branch prediction bits correctly predicts the branch resolution outcome; and

updating the corresponding entry in the selector table to a second logic value when the at least one of the second set of branch prediction bits correctly represents the branch resolution outcome.

36. The method of Claim 35 and further comprising the steps of:

determining if at least one bit of both the first and second sets of branch history bits correctly predict the branch resolution outcome;

maintaining the current value of corresponding bits in the corresponding selector table entry when the at least one bit of both the first and second sets of branch prediction bits correctly predict the branch resolution outcome;

determining if at least one bit of both the first and second sets of branch prediction bits incorrectly predict the branch resolution outcome; and

maintaining the current value of corresponding bits in the corresponding selector table entry when the at least one bit of both the first and second sets of branch history bits incorrectly predict the branch history outcome.

37. The method of Claim 35 and further comprising the steps of :

determining whether at least one bit of both the first and second sets of branch prediction bits correctly predict the branch resolution outcome;

maintaining the current value of corresponding bits in the corresponding selector table entry when at the least one bit of both the first and second sets of branch prediction bits correctly predict the branch resolution outcome; and

updating the current selector table entry to a logic value associated with the fetch-based branch history table when neither of corresponding bits of the first and second sets of branch prediction bits correctly predicts the branch resolution outcome.

38. The method of Claim 34 wherein said step of accessing the fetch-based branch history table comprises the substep of generating an address from at least some bits of a branching instruction and bits retrieved from a history register.

39. The method of Claim 38 wherein the history register comprises a shift register.

40. The method of Claim 39 wherein said method further comprises the steps of updating the shift register by shifting in a prediction bit for each fetch group.